NCP5890

Light Management IC Dedicated for LCD Backlighting and Multi-LED Fun Light Applications

The NCP5890 is part of the Light Management IC (LMIC) family. It is a fully programmable subsystem that manages multiple illumination functions integrated into the silicon.

Features

- 34 V Output Voltage Capability
- Include Three Independent PWM to Control LED Segments
- 2.7 to 5.5 V Input Voltage Range
- 90% Peak Efficiency with 4.7 μH / 150 mΩ Inductor
- Gradual Dimming Built−in
- Integrated Ambient Light Sensing Adjusts Backlight Contrast
- Built−in I2C Address Extension
- Tight 1% I−LED Tolerance
- True Cut Off Function Minimizes Load Leakage Current in Shutdown
- Ultra Thin 0.5 mm QFN16 Package
- This is a PB−Free Device

Typical Applications

- Portable Back Light & Keyboard
- Digital Cellular Phone Camera Photo Flash

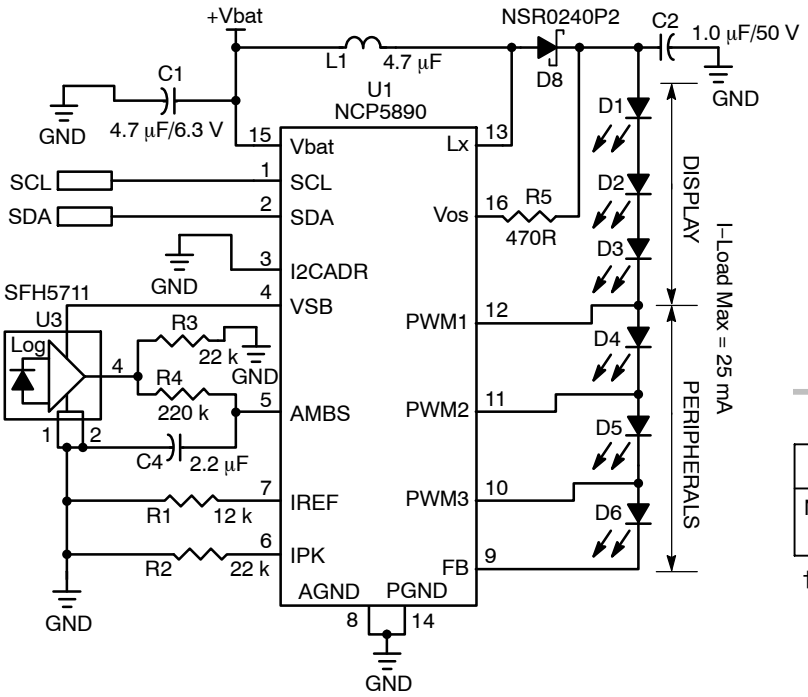

Figure 1. Typical Multiple White LED Application

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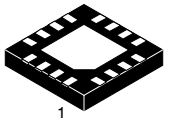
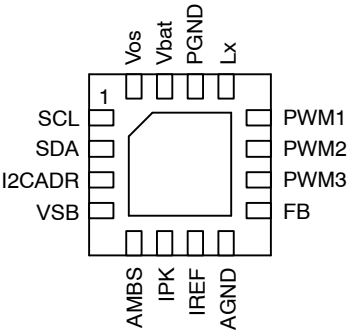


UQFN16
MU SUFFIX
CASE 523AF

MARKING DIAGRAM

5890	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5890MUTXG	UQFN16 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

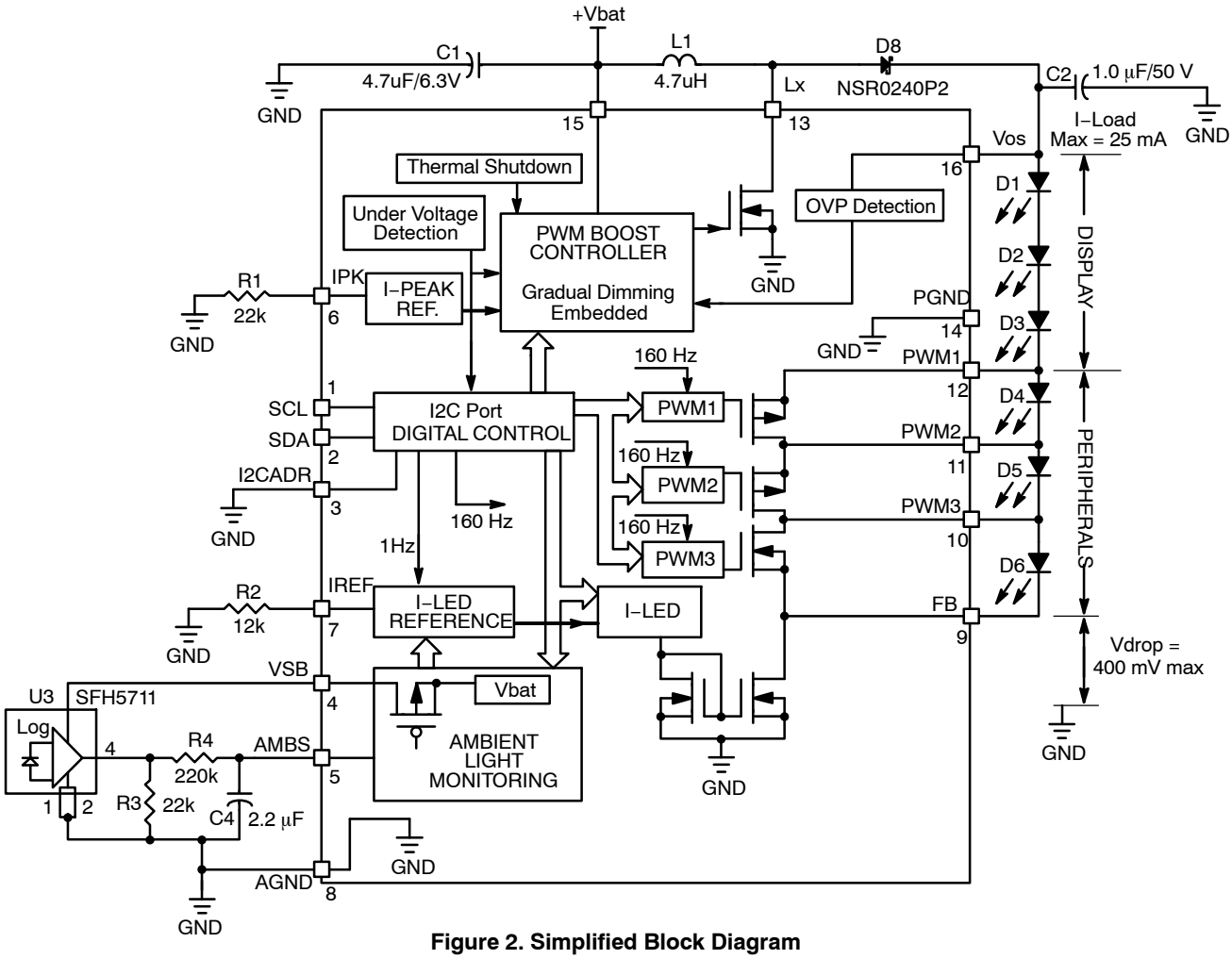


Figure 2. Simplified Block Diagram

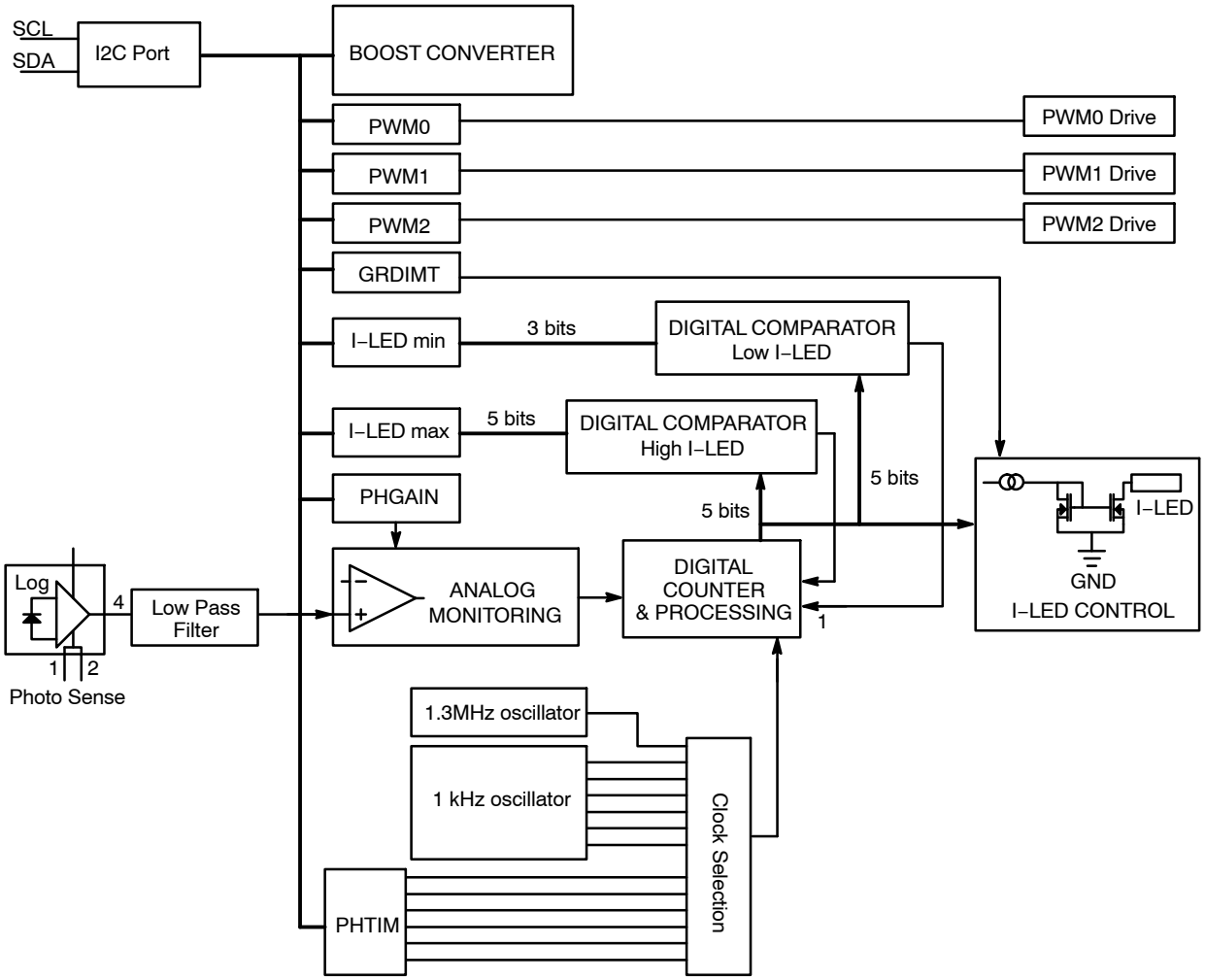


Figure 3. Basic NCP5890 Structure

PIN DESCRIPTIONS

PIN	Name	Type	Description
1	SCL	INPUT, DIGITAL	This pin carries the I2C clock to control the DC/DC converter and is used to set up the output current and the photo sensor. The SCL clock is associated with the SDA signal.
2	SDA	INPUT, DIGITAL	This pin carries the data provided by the I2C protocol. The content of the SDA byte is used to program the mode of operation and to set up the output current.
3	I2CADR	INPUT, DIGITAL	This pin is used to select the I2C address of the NCP5890: I2CADR = Low → address = %0111 0010 = $72 I2CADR = High → address = %0111 0100 = $74 In order to avoid any risk during the operation, the digital levels are intended to be hardwired prior to power up the system.
4	VSB	POWER, OUTPUT	This pin provides a switched voltage, derived from the Vbat supply, to bias the external photo sense. The current capability of this voltage is 2 mA. The VSB switch output is open when the Shutdown mode has been engaged.
5	AMBS	INPUT, ANALOG	This pin senses the voltage developed across the external Photo Bias resistor. Since this is a very high impedance input, care must be observed to minimize the leakage current and the noise that may influence the photo sense analog function. The bias parameters associated with the AMBS pin are reloaded when the chip resumes from Shutdown to Normal operation.
6	I_{PK}	INPUT, ANALOG	This pin provides the inductor peak current during normal operation. In no case shall the voltage at I_{PK} pin be forced either higher or lower than the 1144 mV provided by the internal reference.
7	I_{REF}	INPUT, ANALOG	This pin provides the reference current, based on the internal band−gap voltage reference, to control the output current flowing in the LED. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the LED biases. An external current source can be used to bias this pin to dim the light coming out of the LED. In no case shall the voltage at I_{REF} pin be forced either higher or lower than the 1144 mV provided by the internal reference.
8	AGND	POWER	This pin is the GROUND signal for the analog and digital blocks and must be connected to the system ground. A ground plane is strongly recommended.
9	FB	INPUT, ANALOG	This pin is the current sense of the series arranged LED. The built−in current mirror will automatically adapt the voltage drop across this pin (typically 400 mV).
10	PWM3	INPUT, ANALOG	This pin provides a PWM control of the LED connected between PWM3−FB. The PWM is programmed by the I2C port and preset to zero upon power ON.
11	PWM2	INPUT, ANALOG	This pin provides a PWM control of the LED connected between PWM2. The PWM is programmed by the I2C port and preset to zero upon power ON.
12	PWM1	INPUT, ANALOG	This pin provides a PWM control of the LED connected between PWM1. The PWM is programmed by the I2C port and preset to zero upon power ON.
13	Lx	POWER	The external inductor shall be connected between this pin (drain of the internal Power switch) and Vbat. The voltage is internally clamped at 34 V under worst case conditions. The external Schottky diode shall be connected as close as possible to this pin. See Note 1 for ESR recommendations.
14	PGND	POWER	This pin is the GROUND reference for the DC/DC converter and the output current control. The pin must be connected to the system ground, a ground plane is strongly recommended.
15	VBAT	INPUT, POWER	Input Battery voltage to supply the analog , the digital blocks and the main Power switch driver. The pin must be decoupled to ground by a 10 μF ceramic capacitor.
16	Vos	INPUT, POWER	This pin senses the output voltage supplied by the DC/DC converter. The Vos pin must be bypassed by 1.0 μF/50 V ceramic capacitor located as close as possible to the pin to properly bypass the output voltage to ground. The circuit will not operate without such bypass capacitor connected to the Vos pin. The output voltage is internally clamped to 34 V maximum in the event of a no load situation. NOTE: Due to the very fast dV/dt transient developed during the operation, using a low pass filter is strongly recommended as depicted in the schematic diagram Figure 1.

1. Using low ESR ceramic capacitor and low DCR inductor is mandatory to optimize the DC/DC efficiency

MAXIMUM RATINGS (Note 2)

Symbol	Rating	Value	Unit
V_{BAT}	Power Supply	−0.3 < V < 7.0	V
V_{LX}	Output Switching Voltage	34	V
SCL, SDA	Digital Input Voltage Digital Input Current	−0.3 < V < V_{BAT} 1	V mA
ESD	Human Body Model: R = 1500 Ω, C = 100 pF (Note 3) Machine Model	2 200	kV V
P_D $R_{\theta jc}$ $R_{\theta ja}$	UQFN16 package − Power Dissipation @ T_A = +85°C (Note 4) − Thermal Resistance Junction to Case − Thermal Resistance Junction to Air	300 50 130	mW °C/W °C/W
T_A	Operating Ambient Temperature Range	−40 to +85	°C
T_J	Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature Range	−65 to + 150	°C
	Latch−up current maximum rating per JEDEC standard: JESD78.	±100	mA

2. Maximum electrical ratings define the values beyond which permanent damage(s) may occur internally to the chip whatever the operating temperature may be.
3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
4. The maximum package power dissipation limit must not be exceeded.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION: (Typical values are referenced to Ta = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted),operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
15	V_{bat}	Power Supply	2.7		5.5	V
15	V_{UVLO}	Power Supply Input Voltage (See Figure 22)	2.0	2.2	2.4	V
15	V_{UVLOHY}	Under Voltage Hysterisis, negative going slope	150		270	mV
13	I_{out}	Continuous load DC current, Vout pin @ 3.0 V < Vbat < 5.5 V, Cout = 1.0 μF	25			mA
13	Isw	Output Leakage Current (Lx pin) @ Iout = 0, Vout = 35 V			200	nA
	Vout	Output Voltage Compliance (OVP)	30	32	34	V
	$Vout_{HY}$	OVP Output Voltage Hysterisis	1.0		1.8	V
	Tstart	DC/DC Start time (Cout = 1.0 μF) 3.0 V < Vbat = nominal < 5.5 V from last ACK bit to full load operation		600		μs
15	I_{stdb}	Stand By Current, Vbat = 3.6 V, Iout = 0 mA @SCL = SDA = H (no port activity)			1.0	μA
15	I_{op}	Operating Current, @ Iout = 0 mA, Vbat = 3.6 V		2.0		mA
13	I_{PK}	Maximum Inductor Peak Current @ R = 13 kΩ	−10%	855	+10%	mA
13	I_{TOL}	Output Current Tolerance @Vbat = 3.6V, I_{LED} = 10 mA −25°C < T_A < 85°C		±1		%
13	Fpwr	Boost Operating Frequency (0°C < T_A < 85°C)	1.13	1.3	1.47	MHz
	T_{SD}	Thermal Shutdown Protection		160		°C
	T_{SDH}	Thermal Shutdown Protection Hysteresis		30		°C
	E_{PWR}	Efficiency @ Vbat = 3.6 V, ESR ≤ 150 mΩ Coilcraft = LPO3310−472ML, Cout = 1.0 μF I−LED = 10 mA, Vf = 2.85 V I−LED = 25 mA, Vf = 3.4 V (Note 6)		75 80		% %
	$R_{DS(on)}$	Power Switch NMOS $R_{DS(on)}$		500		mΩ

6. Note 1: using low DCR inductor with low eddy current losses is mandatory to get the high efficiency operation

ANALOG SECTION: (Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
7	I_{REF}	Reference Current @ Vref = 1144 mV (Note 8)	1		100	μA
6	I_{PK}	Reference Current @ Vref = 1144 mV (Note 8)	1		100	μA
	k_{ref}	Reference Current to ILED peak current ratio		250		
	k_{pk}	Reference Current to Inductor peak current ratio		9700		
7	V_{REF}	Reference Voltage (Note 8)	−3%	1144	+3%	mV
6	V_{REFK}	Reference Voltage (Note 8)	−10%	1144	+10%	mV
9	V_{FB}	Feedback Voltage @ ILED = 25 mA (Note 9)		425		mV
	M_{DCY}	Boost Operating Maximum Duty Cycle (0°C < T_A < 85°C)	90	94		%
9	I_{LKGM}	Current Mirror Leakage Current			200	nA
10, 11, 12	Fpwm	Low Frequency PWM Clock (derived from F_{pwr}/8192)	140	160	185	Hz
	F_{LF}	Low Frequency Clock (derived from F_{pwr}/8192)	0.6		20	Hz
4	V_{VSD}	Photo sense bias supply @ Ibias = 1 mA	2.5		Vbat	V
4	R_{VSD}	Photo sense bias supply internal impedance		30		Ω
4	I_{SDUSD}	Photo sense leakage current (Note 11)			100	nA
	$G_{AMB0.25}$	Photo sense internal Gain 1/4		0.25		
	$G_{AMB0.50}$	Photo sense internal Gain 1/2		0.5		
	G_{AMB01}	Photo sense internal Gain 1		1		
	G_{AMB02}	Photo sense internal Gain 2		2		
	G_{AMB04}	Photo sense internal Gain 4		4		
5	V_{iph}	Photo sense input voltage (Note 10)			1.5	V
10	BVpwm2	Breakdown Voltage pin 10 to pin 10 (Note 11)	9			V
11	BVpwm2	Breakdown Voltage pin 11 to Pin 12 (Note 11)	9			V
12	BVpwm1	Breakdown voltage pin 12 to GND (Note 11)	9			V

7. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
8. The external circuit must not force the $I_{REF\ or}$ I_{PK} pin voltage either higher or lower than the specified voltage. The reference voltage applies to both I_{REF} and I_{PK} pins.
9. This parameter guarantees the function for production test purposes.
10. The ambient sense linearity is guaranteed when the voltage at the output of the internal amplifier is limited to 1.5 V. This voltage is equal to the input voltage times the programmed gain. Beyond this value, the operational amplifier is in the saturation region and the linearity is no longer guaranteed.
11. Parameter guaranteed by design, not tested in production.

DIGITAL PARAMETERS SECTION: (Typical values are referenced to Ta = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
1	F_{SCK}	Input I2C clock frequency			400	kHz
1,2	V_{IH}	Positive going Input High Voltage Threshold, SCL, SDA signals	1.6		V_{BAT}	V
1,2	V_{IL}	Negative going Input High Voltage Threshold, SCL, SDA signals	0		0.4	V
2	C_{IN}	SDA Input Capacitance		10	15	pF
3	V_{IHD}	I2C address extension	Vbat*0.7		Vbat+0.3V	V
3	V_{ILD}	I2C address extension	0		0.3	V

NOTE: Digital inputs undershoot < − 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}

DC/DC OPERATION

The boost converter is based on a PWM structure to generate the output voltage necessary to drive the series arranged LED. The system includes an open load detection to avoid over voltage situation when the LED are disconnected from the Vout pin. A built−in circuit prevent high inrush current when the system is powered.

The ILED is regulated by means of a built−in current mirror controlled by the digital content of the ILEDREG register. With a typical 1.3 Mhz operation frequency, the converter can run at full power with a tiny 4.7 μH inductor. However, care must be observed, at DCR level, to optimize the total DC/DC conversion efficiency. In particular, the ferrite material shall have limited eddy current losses at high frequency. Depending upon the type of material, the eddy losses in the inductor can range from a low 40 mW to a high 250 mW under the same bias and load conditions.

The ILED current is regulated by the means of internal current mirror connected to the FB pin. The voltage at this pin can vary between a low 100 mV to a 1.5 V maximum, depending upon the ILED current amplitude. Typically, the FB voltage will be 425 mV under normal operation.

Table 1. Recommended Inductor Manufacturers

Part Number	Manufacturers
LPO3310−472ML	COILCRAFT
VLS3010T−4R7MR80	TDK

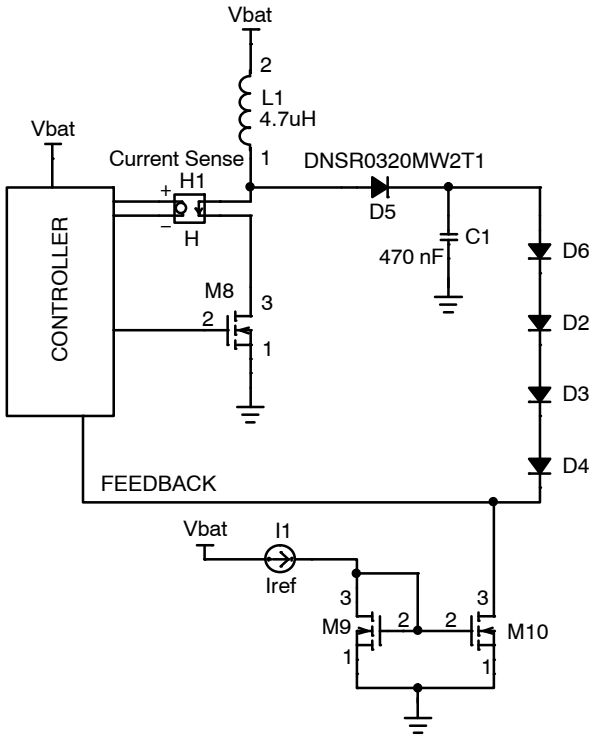


Figure 4. Simplified Boost Structure

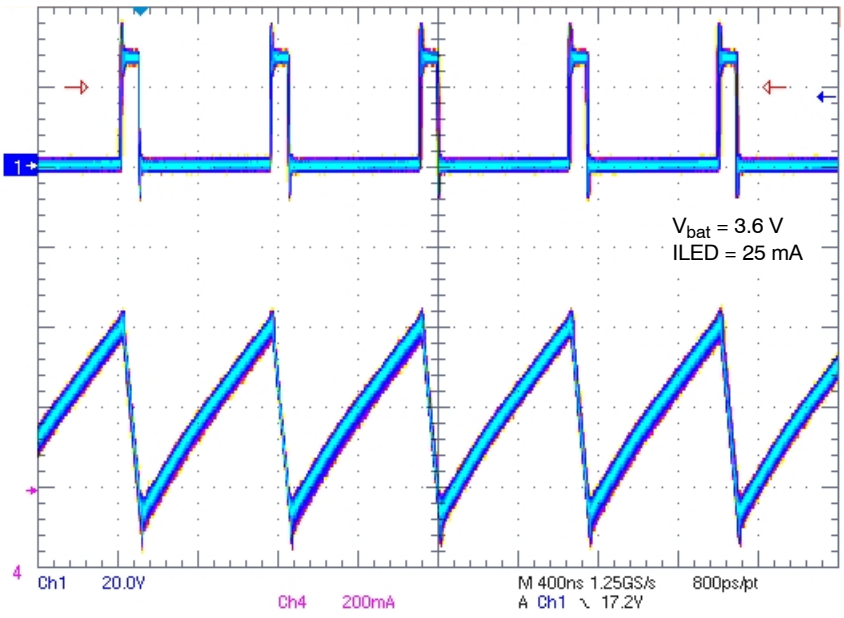


Figure 5. Typical Switching Operation

Although the total ohmic resistance plays an important role in the losses developed in the converter, the switching losses are key when the operating frequency is beyond a few kilohertz range. To minimize such losses, the internal power NMOS is designed to minimize the dI/dt, thus minimizing the I*V crossing time. As a consequence, the slope of the positive going voltage −VLX− present at the Lx pin is very fast as well and an overshoot is created since the Schottky rectifier has an intrinsic turn-on time: the voltage keeps going until the diode turns−on, clamping the VLX voltage at the output value. Such a mechanism is depicted in Figure 6. The proposed Schottky, depicted in the schematic Figure 1, is a good alternative to minimize such an overshoot.

On the other hand, the same overshoot is propagated to the Vout voltage when the system operates under open load condition. As a consequence, it is strongly recommended to implement a simple filter, built with a small footprint resistor, to makes sure that no any uncontrolled operation of the high sensitive pin Vos will happen under the worst case conditions: see Figure 1, resistor R5.

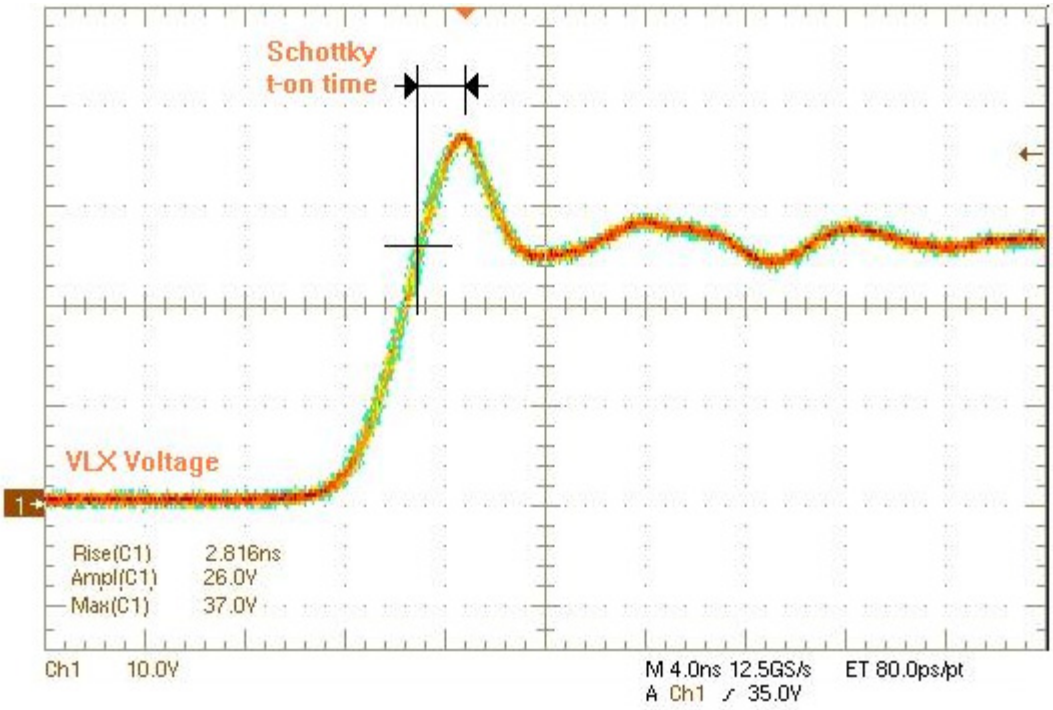


Figure 6. Typical Turn On Time of the Schottky Rectifier

I2C Protocol

The standard I2C protocol is used to transfer the data from the MCU to the NCP5890. Leaving aside the Acknowledge bit, the NCP5890 chip does not return data back to the MCU.

The physical address of the NCP5890 can be selected as 0111 001X or 0111 010X (the X being the Read / Write identifier as defined by the I2C specification) depending upon the digital status present at the I2CADR pin:

I2CADR = Low → address = %0111 0010 = $72

I2CADR = High → address = %0111 0100 = $74

In order to avoid any risk during the operation, the digital level at the I2CADR pin must be hardwired either to GND or to Vbat prior to power up the system.

The first byte of the I2C frame shall be selected address ($72 or $74) when a Write is send to the chip.

To set up a new output current value, a full frame will be sent by the MCU. The frame contains three consecutive bytes and shall fulfill the I2C specifications (see Figure 7):

- First byte: I2C address, write → $72 (assuming I2CADR = Low)
- Second byte: register selection → %0000 XXXX = internal register address
- Third byte: DATA → %XXXX XXXX = function / output current value

An infinite number of register selection / data pair can be send on the I2C port once the physical address has been decoded (see Figure 8). The transmission ends when the STOP signal is send by the SCL/SDA digital code.

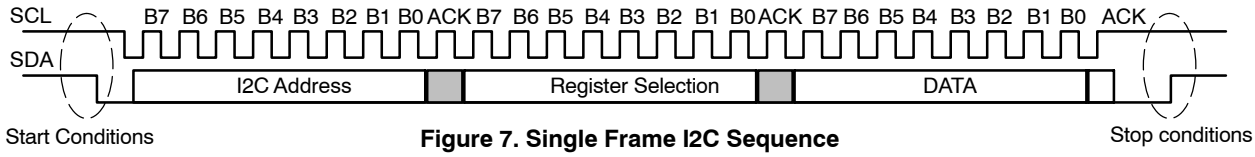


Figure 7. Single Frame I2C Sequence

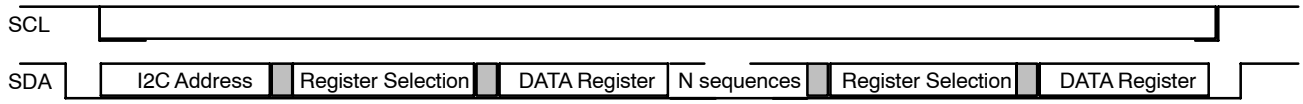


Figure 8. Multi Frames I2C Sequence

On the other hand, although the chip does not handle the Read operation, care must be observed since sending a Read command ($73 or $75) is equivalent to a Write command and the selected register will be updated accordingly.

Registers Setup Selection

The Register Selection follows the I2C address of a new frame and must be followed by the DATA Register. The content of the Register Selection byte is not stored into the chip and a new one must be sent for every DATA upload.

The last code $0F is reserved for ON Semiconductor to control the manufacturing test and access to this register is not permitted outside the ON Semiconductor final test facilities.

Shutdown and True Cut−off

To shutdown the device the user must write $00 in Register Selection. When in shutdown condition, FB pin is turned in impedance and truly isolates the load from the battery. The NCP5980 is immediately turn on when one of the Register Selection from $01 to $0F is active to point a given DATA Register.

Table 2. Register Selection

Register Functions	Register	Address
Shutdown the chip	SDN	$00
Select I−LED current setup and immediate LED update	ILEDREG[4..0]	$01
Select I−LED target Gradual Dimming command UP	GDIM−UP[4..0]	$02
Select I−LED target Gradual Dimming command DOWN	GDIM−DWN[4..0]	$03
Set Timing & Start gradual Dimming Sequence	TDIM[4..0]	$04
Select PWM0 register	PWM0[4..0]	$05
Select PWM1 register	PWM1[4..0]	$06
Select PWM2 register	PWM2[4..0]	$07
Set up Photo sense input stage gain	PHGAIN[4..0]	$08
Set up Photo Sense I−LED minimum value	PHMIN[3..0]	$09
Set up Photo Sense timing	PHCLK[5..0]	$0A
RFU		$0B
RFU		$0C
RFU		$0D
RFU		$0E
Reserved for manufacturing test: *do not access*	FTEST[7..0]	$0F

ILED Current

The ILED current depends upon the reference current (I_{REF} pin) and the digital contents of the ILEDREG register. The I2C port is used to program the ILED current by writing to the ILEDREG register. The load current is derived from the 1144 mV reference voltage associated to the external resistor connected across I_{REF} pin and Ground (see Figure 9). The maximum ILED current is given by the internal current mirror ratio (multiplier − k−) equal to 250. In other words, to get a 25 mA maximum, with a 100% full range (ILEDREG = $1F), the reference current should be 25 mA/250 = 100 μA. This current is used to calculate the resistor connected between the IREF pin and GND: R_{REF} = 1.144 / 100e−6 = 11.44 kΩ. In any case, no voltage shall be forced at I_{REF} pin, either downward or upward.

The tolerance of the external resistor must be 1% or better, with a 100 ppm thermal coefficient, to get the expected overall tolerance.

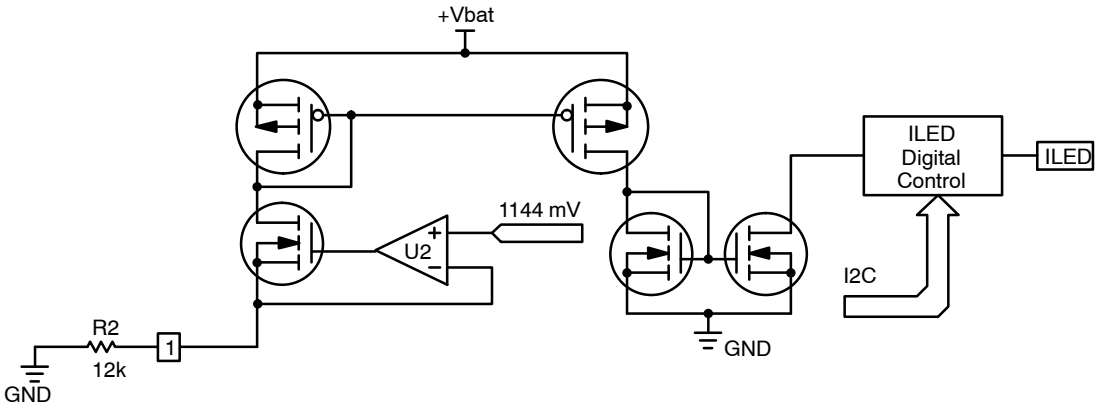


Figure 9. Basic Reference Current Source

NOTE: The I_{REF} pin must never be biased by an external voltage higher than 1144 mV.

The ILED current is given by Table 3 as a percentage of the maximum programmed ILED value (100% will give 25 mA when Iref = 100 μA).

Table 3. Output Current (%) versus ILED Step Value

Step # ($)	Iout %	Step # ($)	Iout %	Step # ($)	Iout %	Step # ($)	Iout %
00	0.00	08	1.40	10	6.24	18	27.48
01	0.42	09	1.70	11	7.52	19	33.03
02	0.49	0A	2.00	12	9.11	1A	39.72
03	0.57	0B	2.42	13	10.92	1B	47.72
04	0.72	0C	2.99	14	13.08	1C	57.47
05	0.87	0D	3.63	15	15.80	1D	69.18
06	1.02	0E	4.35	16	18.97	1E	83.20
07	1.17	0F	5.22	17	22.86	1F	100.00

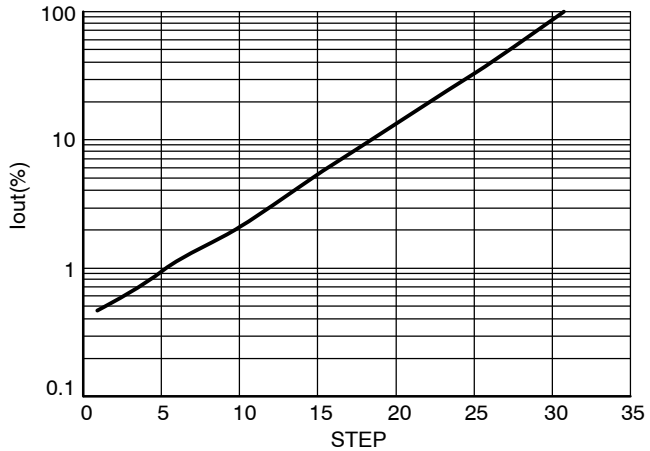


Figure 10. Typical Iout (%) versus ILED Step Value

$01 ILEDREG[0..4] I–LED Peak Current

	B7	B6	B5	B4	B3	B2	B1	B0
step	–	–	–	ILED16	ILED8	ILED4	ILED2	ILED1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU
Bits [B4:B0] : ILED peak current setup

Inductor Peak Current

This safety feature is clamping the maximum current allowed in the inductor according to external R_{PCA} resistor, which is connected between IPK input and the ground.

The maximum I_{PK} current is given by the internal current mirror ratio (multiplier − kk −) typically equal to 9700. In other words, to get a 855 mA maximum peak current in the inductor, the reference current should be 850 mA/9700 = 87.6 μA. This current is used to calculate the resistor connected between the I_{PK} pin and GND: R_{REF} = 1.144 / 87.6e−6 = 13 kΩ.

The concept depicted in the ILED current paragraph applies as well and care must be observed to avoid any voltage source connection to the IPK pin.

Gradual Dimming

The purpose of this function is to gradually Increase or Decrease the brightness of the backlight / keyboard LED upon command from the external MCU. The function is activated and controlled by means of the I^2C protocol.

The period (either upward or downward) is equal to the time defined for each step, multiplied by the number of steps. The number of step is derived from the value associated with the target current.

To operate such a function, the MCU will provide two information:

1. The target current level (either upward or downward)
2. The time per step

When a new gradual dimming sequence is requested, the output current changes, according to the exponential curve, from the existing start value to the end value. The end current value is defined by the contents of the Upward (GDIM−UP) or Downward (GDIM−DWN) register, the width of each step is defined by the TDIM register, the number of steps being in the 1 to 32 range ($00 to $1F). In the event of a software error, the system checks that neither the maximum output current (25 mA), nor the zero level are forced out of their respective bounds. Similarly, software errors shall not force NCP5890 into an uncontrolled mode of operation.

The dimming is built with 32 steps and the time delay encoded into DATA register which is the third byte upload by I^2C transmission.

When the gradual dimming is not requested (register selection = $01), the output current is set up to the level defined by the contents of the related register upon acknowledge of the output current byte.

The gradual dimming sequence must be set up before a new output current data byte is sent to the NCP5890. At this point, the brightness sequence takes place when the new data byte is acknowledged by the internal I^2C decoder. Since the six registers are loaded on independent byte flow associated to the I^2C address, any parameter of the NCP5890 chip can be updated ahead of the next function.

$02 GDIM−UP[4..0] and $03 GDIM−DWN[4..0] Gradual Dimming Target

	B7	B6	B5	B4	B3	B2	B1	B0
ms	−	−	−	ILED5	ILED4	ILED3	ILED2	ILED1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU
Bits [B4:B0] : ILED peak current setup or Gradual Dimming Timing

The number of steps for a given sequence, depends upon the start and end output current range: since the IPEAK value is encoded in the ILEDREG [4:0] binary scale, a maximum of 31 steps is achievable during a gradual dimming operation.

To select the direction of the gradual dimming (either Upward or Downward), one shall set−up the appropriate register before to activate the sequence as depicted in the example here below:

- First Byte = 0111 0000 → I2C address (assuming I2CADR = Low)
- Second byte = 0000 0010 → select an ILED target UPWARD sequence
- Third byte = 0000 1111 → set I−LED = 2.51% of the maximum range
- First Byte = 0111 0000 → I2C address (assuming I2CADR = Low)
- Second byte = 0000 0100 → set Timing and start the sequence
- Third byte = 0000 0010 → set Timing per step = 20 ms/step

$04 TDIM[4..0] Gradual Dimming Time per Step

	B7	B6	B5	B4	B3	B2	B1	B0
ms	0	0	0	200	100	50	25	12.5
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU
Bits [B4:B0] : Gradual Dimming Timing

NOTE: bit B0 = 2^14/F, with F = operating frequency (1.3 MHz typical)

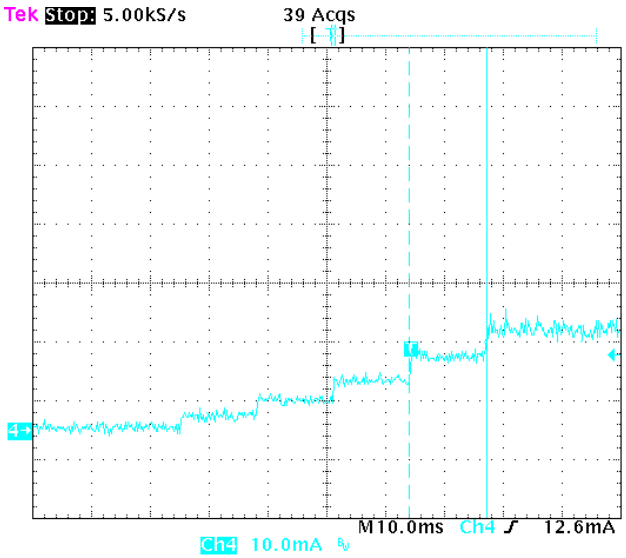


Figure 11. Typical Gradual Dimming UPWARD

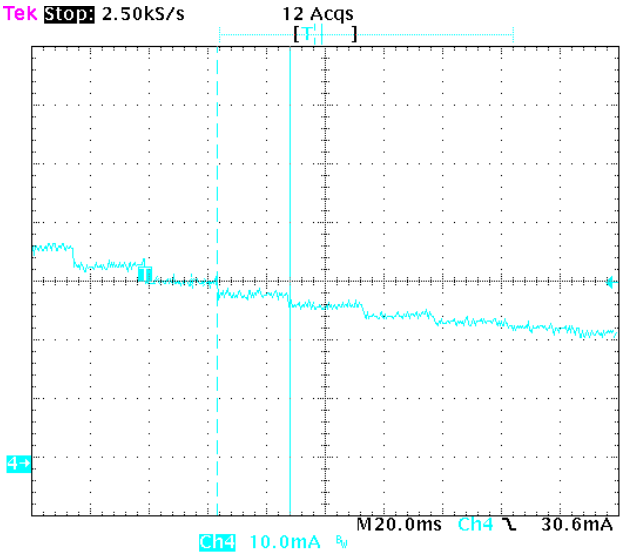


Figure 12. Typical Gradual Dimming DOWNWARD

Keyboard Dimming

The keyboard shares the same I−LED peak current with the backlight, but the built−in PWM structure makes possible a dynamic independent control of three sets of LED. Each PWM is associated with a register, the IC port being used to update the pulse modulation as requested by the application.

$05 PWM0[4..0] PWM0 Modulation

	B7	B6	B5	B4	B3	B2	B1	B0
%	–	–	–	50	25	12.5	6.25	3.125
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU, **Bits [B4:B0] :** PWM0 setup

$06 PWM1[4..0] : PWM1 Modulation

	B7	B6	B5	B4	B3	B2	B1	B0
%	–	–	–	50	25	12.5	6.25	3.125
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU, **Bits [B4:B0] :** PWM1 setup

$07 PWM2[4..0] : PWM2 Modulation

	B7	B6	B5	B4	B3	B2	B1	B0
%	–	–	–	50	25	12.5	6.25	3.125
RESET	0	0	0	0	0	0	0	0

Bits [B7:B5] : RFU, **Bits [B4:B0] :** PWM2 setup

Ambient Light Control

The ambient light can be monitored, by an extra photo diode, to automatically adjust the I−LED peak current as a function of the ambient light. A dedicated I2C command is used to activate or de−activate this function. On the other hand, the end user shall set up the maximum I−LED current by means of an I2C command. The photo sense is automatically de−activated when an I2C command is send through the port, and resume to the pre−programmed status when the I2C command is completed.

The concept is based on analog monitoring of the I−LED current and the photo sense feedback, associated to a Up/Down counter to properly setup the contrast at display level. The photo sense action is bounded by two limits:

- upper I−LED as defined by the end user: the photo sense cannot increase the I−LED above such a limit
- lower I−LED as defined by the end user: the photo sense cannot reduce the back light current to zero.

When the photo sense activates the counter (in either direction), a selectable low frequency clock drives the counter, yielding a smooth and slow brightness variation.

The 100 Hz noise, coming from standard fluorescent tubes, is filter out by means of an external network built between the photo sensor and the AMBS pin. Generally speaking, such a filter is built with a RC network designed to cope with the electrical performances of the selected photo sense. As a consequence, the AMBS pin is biased by a low level voltage signal and processed accordingly the ambient light control structure: see Figure 16.

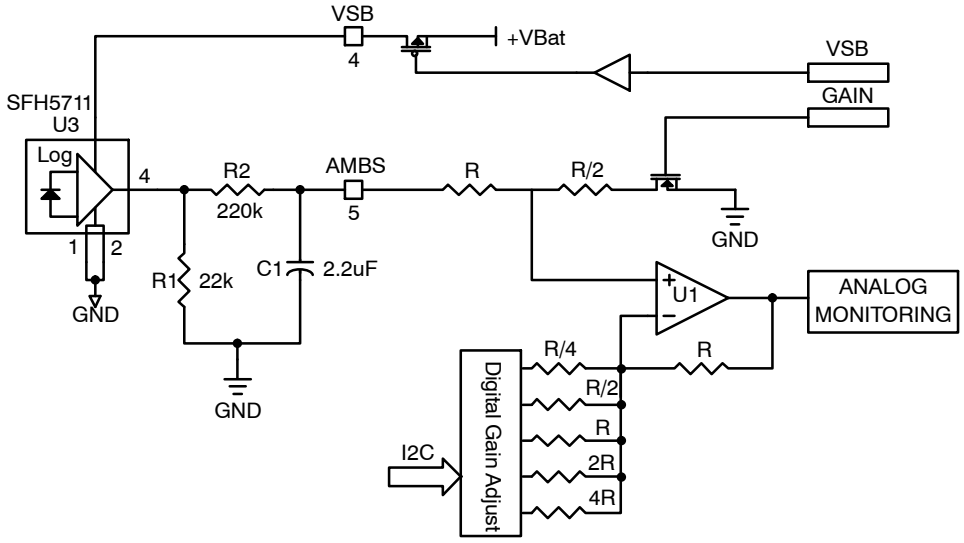


Figure 13. Basic Photo Sense Input Circuit

Since several types of photo sensor can be used in the final application, provisions have been taken into account to dynam−ically adjust the gain of the photo current. Such capability is carried out by the internal register loaded through the I2C port.

$08 PHGAIN[0..4][7]

	B7	B6	B5	B4	B3	B2	B1	B0
	VSD	−	−	PHG5	PHG4	PHG3	PHG2	PHG1
RESET	0	0	0	0	0	0	0	0
Gain				4	2	1	0.50	0.25

Bit [B7] : Photo sense VSD bias control

B7 = 0 → VSD disconnected, photo sense function de−activated

B7 = 1 → VSD connected, photo sense function activated

Bits [B6:B5] : RFU

Bits [B4:B0] : Photo sensor gain adjust

The photo sensor no longer influences the I−LED when the gain is setup to $00. On the other hand, the five bits can be digitally combined to get different gain in the range 0 to 7.75.

When the photo sense returns a lower ambient light level in comparison to the maximum level set up by the user, the I−LED decreases with a timing defined by an I2C command. Such a timing is derived from the Low Frequency clock and selected by the PHTIM register (see Figure 14).

$0A PHTIM[0..5]

	B7	B6	B5	B4	B3	B2	B1	B0
	–	–	PHT6	PHT5	PHT4	PHT3	PHT2	PHT1
RESET	0	0	0	0	0	0	0	0

Bits [B7] : RFU
Bits [B6] : RFU
Bits[B5:B0] :
PHT1 = T = 50 ms/step
PHT2 = T = 100 ms/step
PHT3 = T = 200 ms/step
PHT4 = T = 400 ms/step
PHT5 = T = 800 ms/step
PHT6 = T = 1600 ms/step
Note: the bits cannot be combined to generate a different timing.

In addition, the positive and negative slopes of the I-LED current are intentionally different. In order to generate a smooth transition of the backlight from maximum toward the minimum calculated by the photo sense, the timing of the negative going slope is twice the timing of the positive going slope.

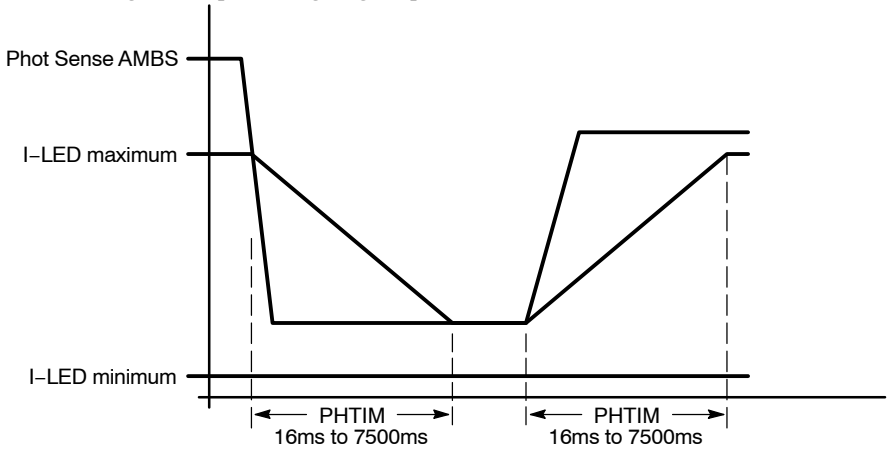


Figure 14. Basic Photo Sense Timing

The rise and fall time of the I−LED current are programmable (according to the PHTIM register contain). The timing is defined by the PHTIM[B5:B0] bits multiplied by the number of steps necessary to reduce / increase the I−LED form one value to the next limit.

On the other hand, the I−LED cannot be reduce to zero during the Photo sense operation: the contain of the PHMIN[B3:B0] register limits the low end current when the photo sensor is in a dark environment.

$09 PHMIN[0..7]

	B7	B6	B5	B4	B3	B2	B1	B0
step	–	–	–	–	PHM4	PHM3	PHM2	PHM1
RESET	0	0	0	0	0	0	0	0

Bits [B7:B4] : RFU
Bits[B3:B0] : set up the I−LED minimum value, according to the exponential table.

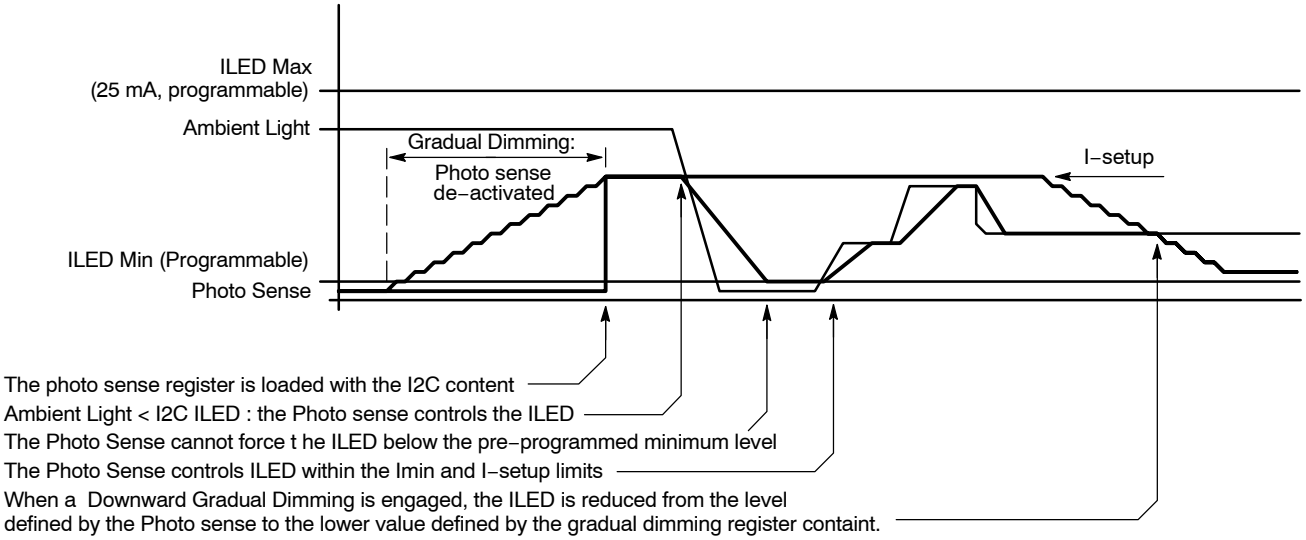


Figure 15. Basic Gradual Dimming and Photo Sense Operation Strategy

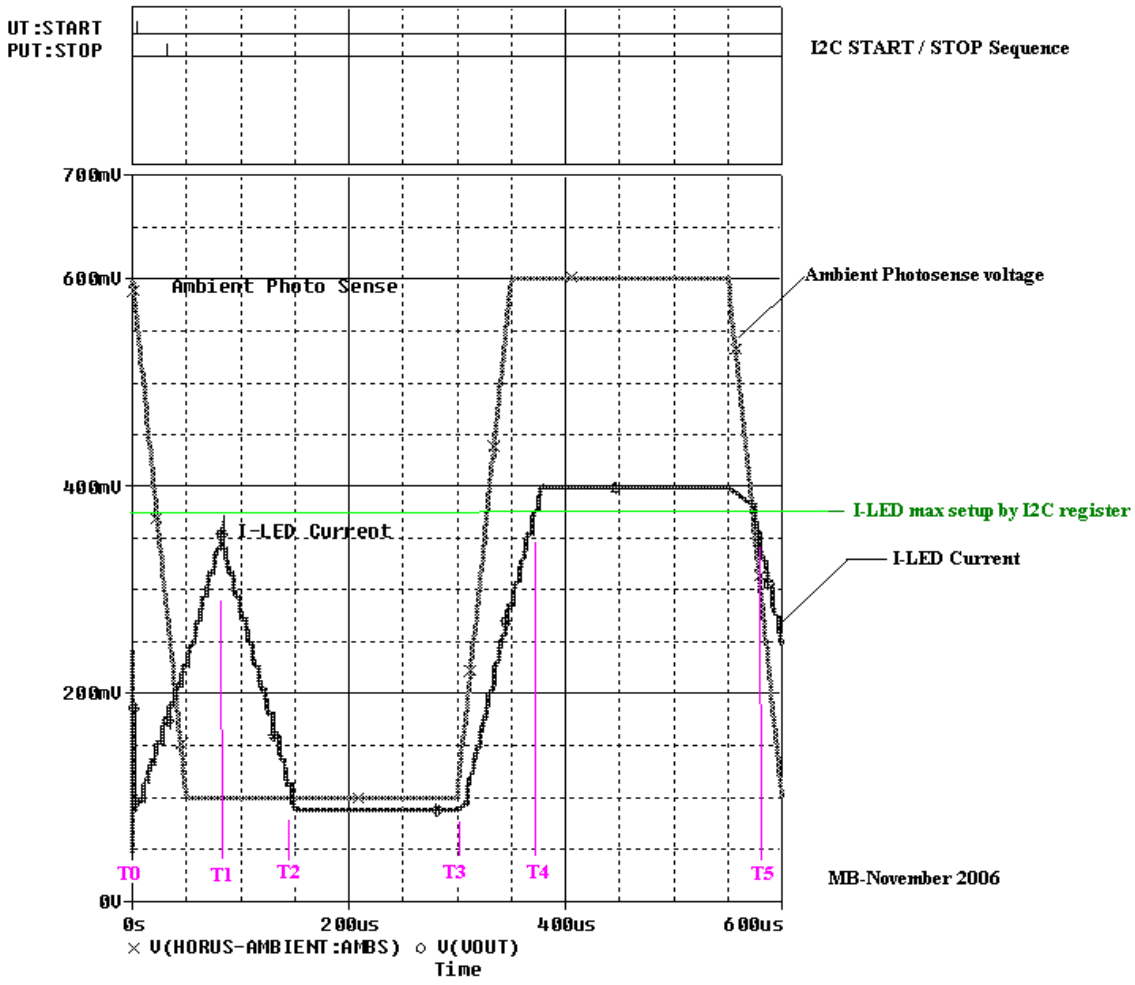


Figure 16. Basic Ambient Photo Sense Regulation (PSPICE simulation)

PWM Sequence

The three PWM can be controlled according to one of the possible sequence depicted in Figure 17. In all cases, the Main Display is powered first.

Strategy #1: the three PWM are fully synchronized and share the same timings, the rise and fall time being identical. At this point, the feedback voltage will rapidly swap from a low 400 mV (normal operation) to the large Vf span coming from the three LED added in series.

Strategy #2: the three PWM share the same rise and fall time, the sequence being synchronized but delayed until the previous LED is at full power (PWM = 100%). This is the most stable sequence, from a human eye stand point, since we have a minimum blinking (one Vf variation only).

Strategy #3: the three PWM share the same rise and fall time but they can be activated independently.

Startegy#4: the three PWM operate randomly: the NCP5890 is capable of operating under such conditions, but care must be observed since such random PWM (as depicted by the circles) might be a stress from a human eye stand point.

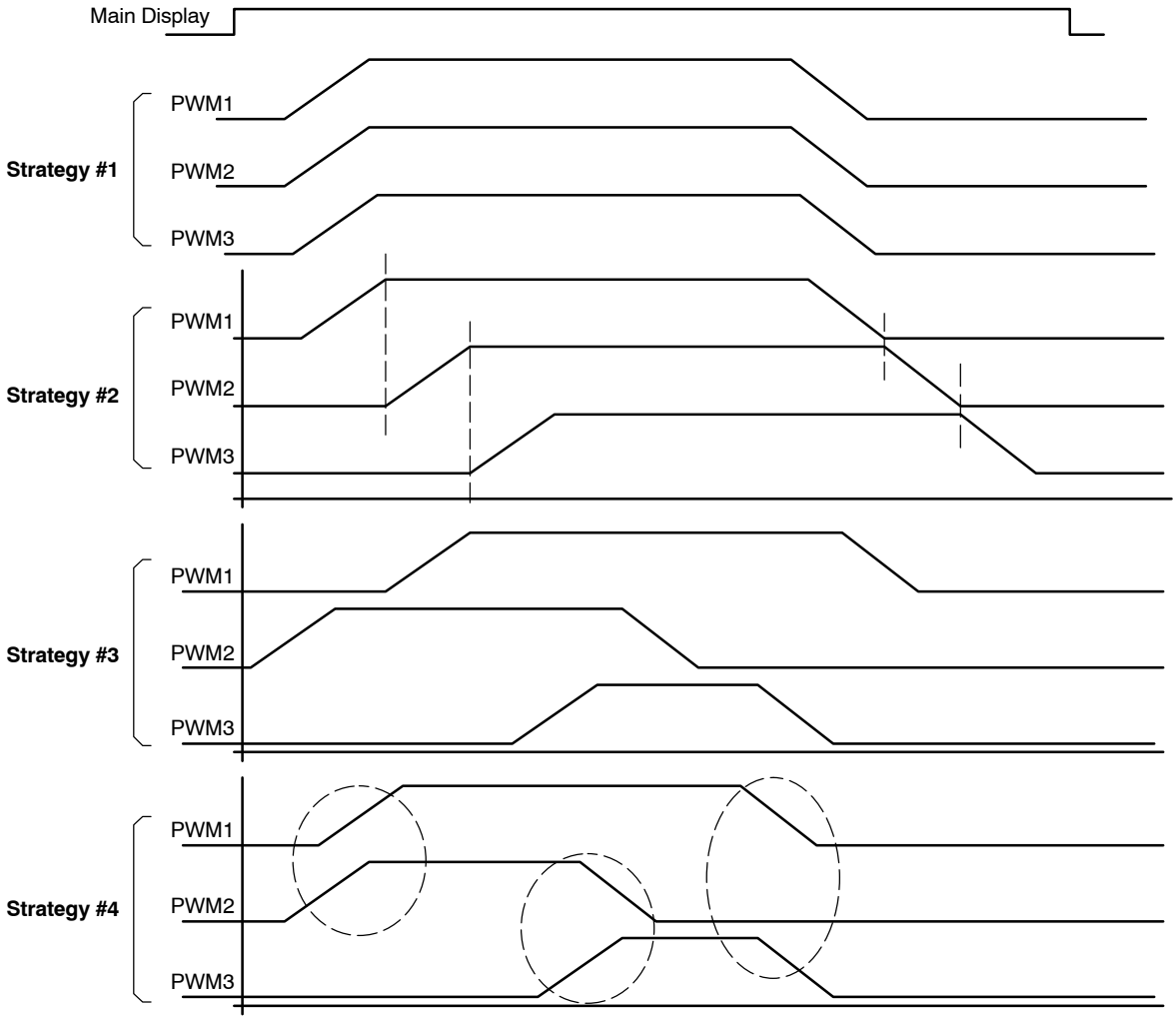


Figure 17. Basic PWM Sequences

In addition, the first PWM structure can control two LED in series as depicted in Figure 18. The next PWM pin is limited to 9.5 V and cannot accommodate over voltage during the operation.

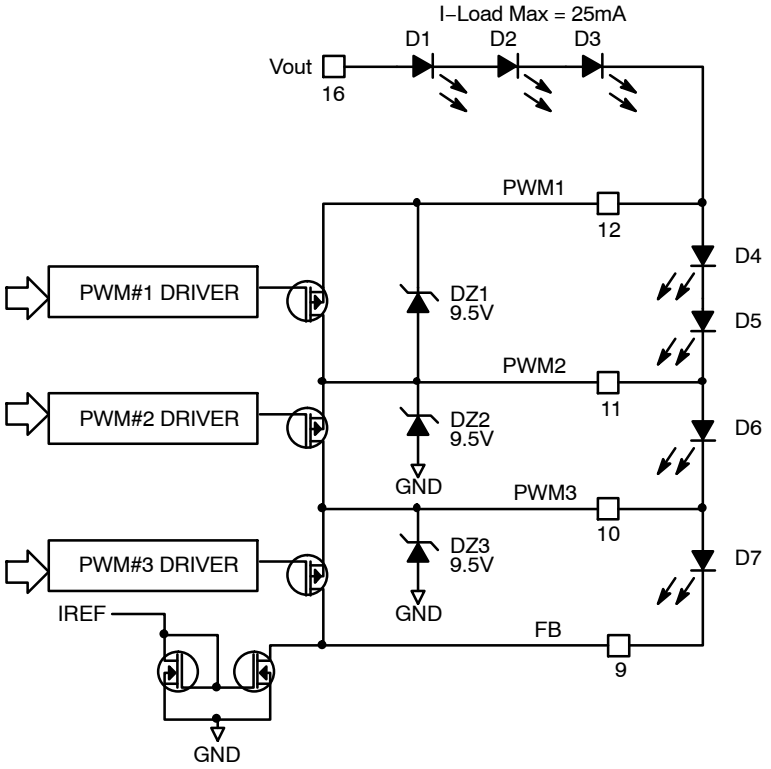


Figure 18. Basic PWM Internal Voltage Clamps

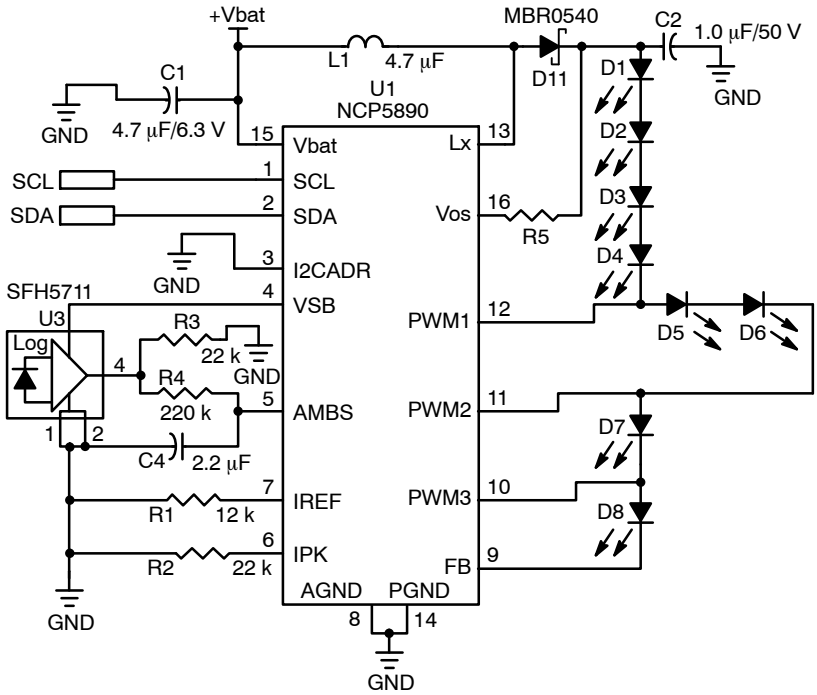


Figure 19. Serial PWM#1 Extension LED

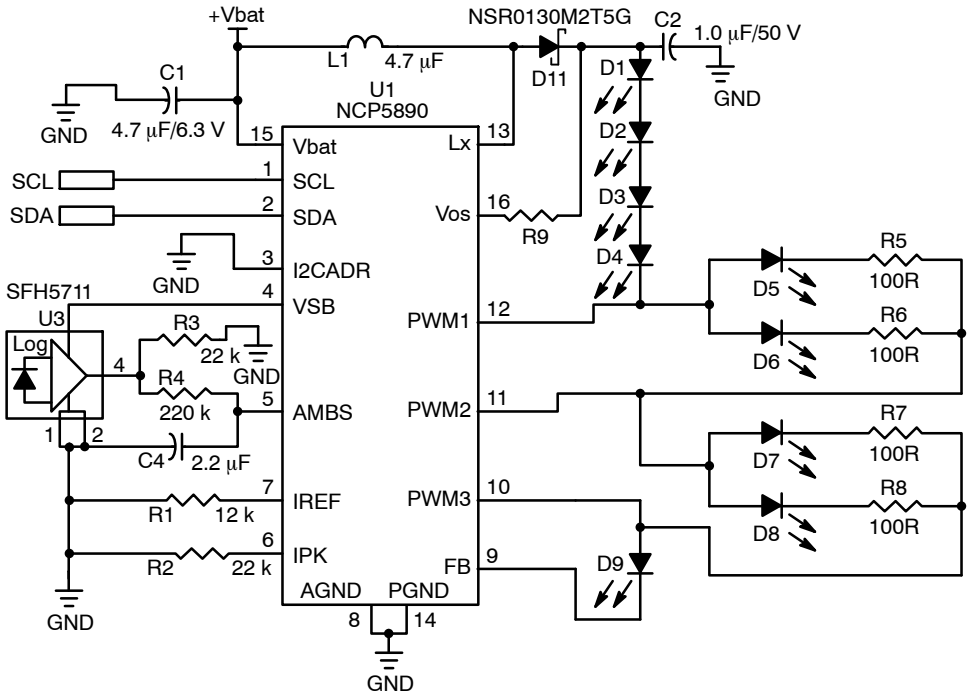


Figure 20. Paralleling Extension LED

ESD PROTECTION CIRCUIT

Depending upon the function of the pin, different circuitry is applied. The basic structures are illustrated in Figure 21.

Although the structures are capable to handle the ESD stresses (as defined by the JEDEC specifications), no current or voltage, either DC or AC, beyond the maximum ratings specifications shall be applied to any pin.

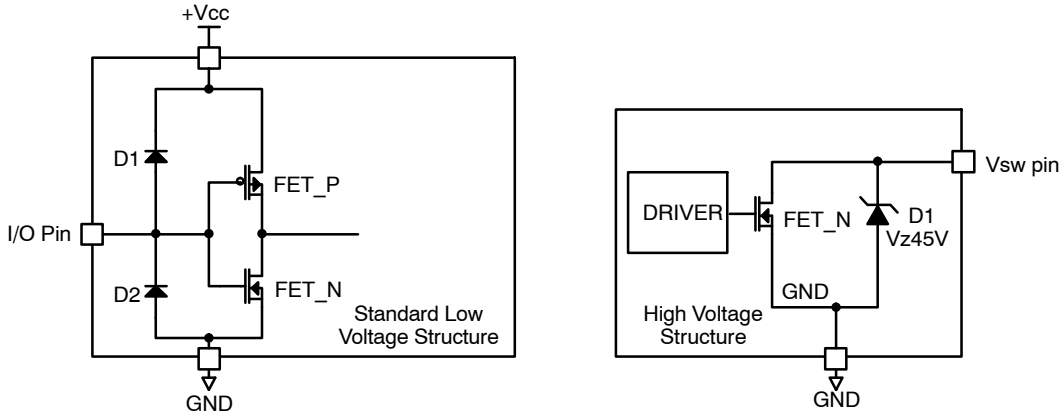


Figure 21. Typical ESD Protection Structures

UNDERVOLTAGE LOCKOUT

The VUVLO circuit is used to disconnect the chip when the input voltage is below the minimum operating value. The system resumes to normal operation when the input voltage increases by the minimum value plus the hysteresis as specified in the data sheet.

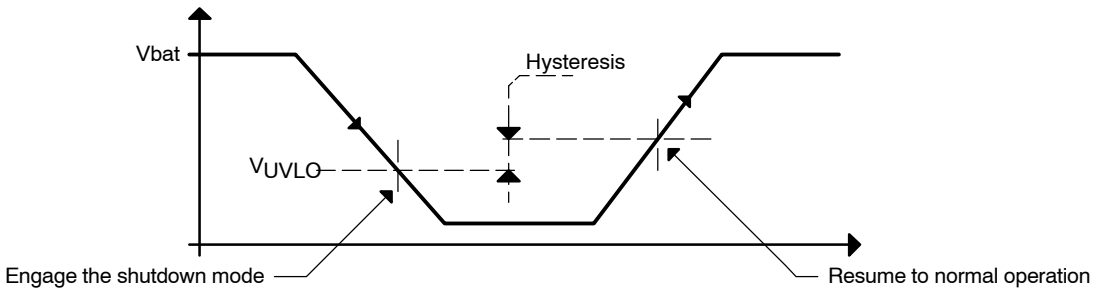
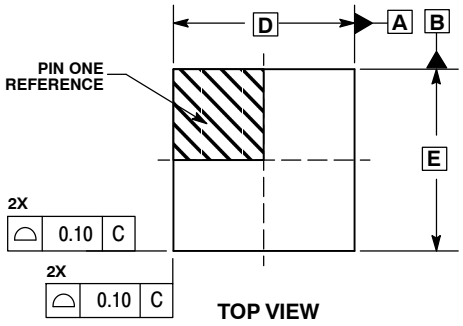
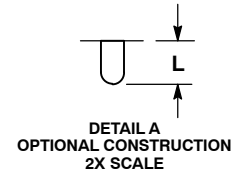


Figure 22. Undervoltage Lockout Basic Mechanism

PACKAGE DIMENSIONS

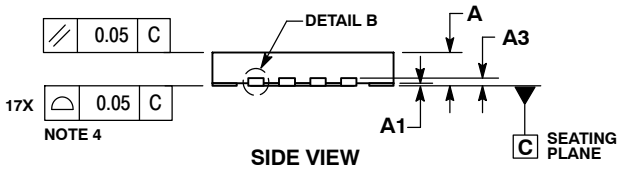
UQFN16 3x3, 0.5P
CASE 523AF−01
ISSUE O

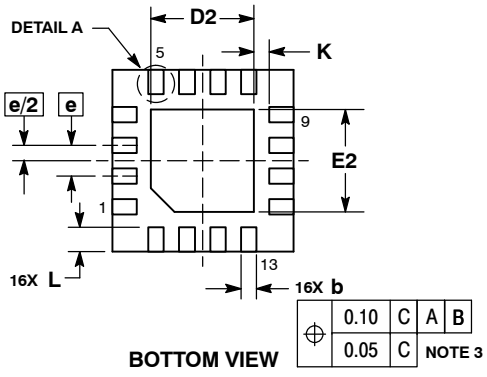




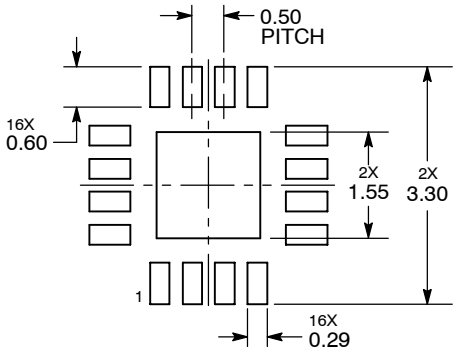
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.60
A1	0.00	0.05
A3	0.127 REF	
b	0.20	0.30
D	3.00 BSC	
D2	1.60	1.80
E	3.00 BSC	
E2	1.60	1.80
e	0.50 BSC	
K	0.20	−−−
L	0.30	0.50





SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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